Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 2. This sheet, which includes Fig. 2, replaces the original sheet including Fig. 2.

Attachments: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

This paper is submitted in reply to the Office Action dated October 22, 2004, within the three-month period for response (since January 22, 2005 is a Saturday, the period for response extends up to and includes January 24, 2005). Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, the drawings were objected to. In addition, claims 6, 8-9, 15 and 17-18 were rejected under 35 U.S.C. §112, second paragraph. Moreover, claims 1-20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,872,963 to Bitar et al.[1]

Applicants respectfully traverse the Examiner's rejections to the extent that they are maintained. Applicants have amended claims 6, 8, 9, 15, 17 and 18 to address the §112 rejections, and added new dependent claim 21. Fig. 2 has been corrected to address the drawing objections. Applicants respectfully submit that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

Now turning to the art-based rejections in the subject Office Action, and more specifically to the rejection of independent claim 1, this claim generally recites a method for yielding a virtual processor within a logically partitioned data processing system, wherein the system supports a plurality of partitions, a first of which includes a plurality of virtual processors that share at least one CPU. The method includes requesting with a yielding virtual processor a yield of the CPU upon which the virtual processor is executing, including designating a target virtual processor from among the plurality of virtual processors. The method also includes switching-in the target virtual processor for execution by the CPU in response to the requested yield.

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[1] The Office Action lists claims 1-6 and 10-15 as rejected under 35 U.S.C. § 102(b); however, Applicants assume that the Examiner rejected claims 1-20 under 35 U.S.C. § 102(b), as all of claims 1-20 are discussed in paragraphs 10-21 of the Office Action.

Applicants respectfully submit that the prior art cited by the Examiner fails to disclose or suggest the above claimed features, including designating or switching-in a specified target virtual processor. The failure of Bitar et al. to teach at least this claimed feature speaks to its disparate purpose. Bitar et al. further fails to disclose any form of yield request that specifies a virtual processor. The objective of Bitar et al. is to achieve switching between user threads without involving the scheduling of virtual processors (col. 5, lines 31-33 and lines 55-58).

Bitar et al. distinguishes between virtual processors and threads at col. 1, lines 27-33. Fig. 2b of Bitar et al. further illustrates this distinction in showing threads 2 mapped to kernel space comprising virtual processors 5 (col. 5, lines 64-65). Fig. 8 likewise shows threads 24.M switched without using kernel space 18 (and associated virtual processors 45). Because Bitar et al. at least fails to teach or suggest the virtual processor feature of claim 1, claim 1 is novel and non-obvious over the cited prior art.

Moreover, Bitar et al. fails to suggest or motivate the features of claim 1, including switching-in a virtual processor. In fact, Bitar et al. teaches away from using a virtual processor, or kernel, and associated scheduling during thread switching for efficiency reasons (col. 5, lines 14-18 and col. 12, line 24). Because Bitar et al. at least fails to teach or suggest switching-in a virtual processor, claim 1 is novel and non-obvious over the cited prior art. Reconsideration and allowance of claim 1, as well as of claims 2-10 which depend therefrom, are therefore respectfully requested.

Independent claim 11 is a computer hardware and software implementation configured to execute method steps similar to those recited in claim 1. Claim 11 is therefore similarly non-obvious and novel over the cited prior art for reasons similar to those discussed in the context of claim 1, and reconsideration and allowance of claim 11, as well as of claims 12-18 and 21 that depend therefrom, are respectfully requested.

Independent claim 19 is basically a program product implementation configured to execute method steps similar to those recited in claim 1. Claim 19 is therefore

similarly non-obvious and novel over the cited prior art, and the reconsideration and allowance of claim 19, as well as of claim 20 that depends therefrom, are respectfully requested.

New claim 21 is patentable by virtue of its dependency on claim 11, in addition to its recital of a virtual processor that includes a schedule. As discussed above, Bitar et al. avoids such schedules when coordinating threads. Claim 21 is therefore novel and non-obvious over the prior art. Consideration and allowance of claim 21 are therefore respectfully requested.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

1/24/05
Date

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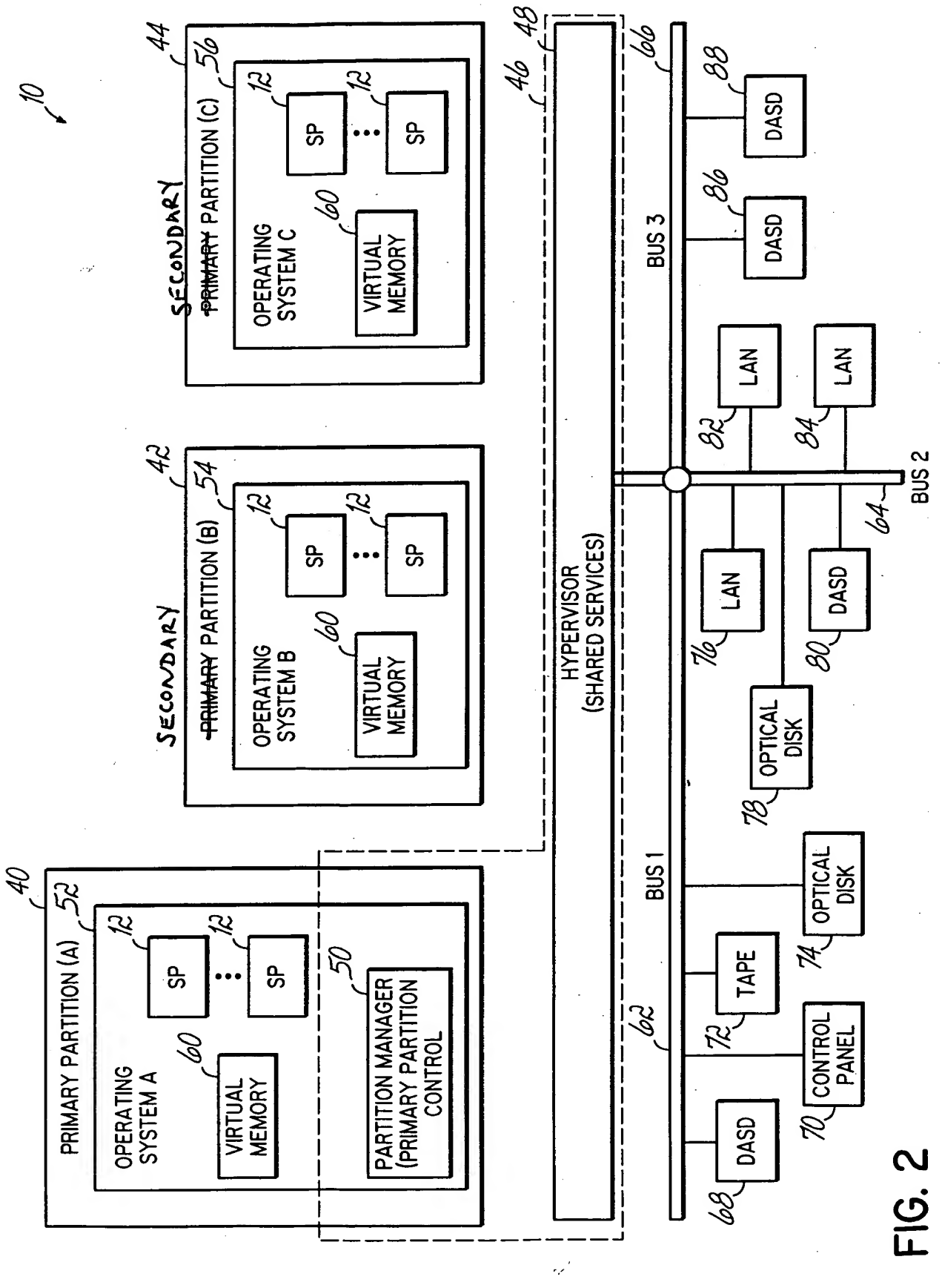

FIG. 2